

Fully integrated GPS LNA IC

Features

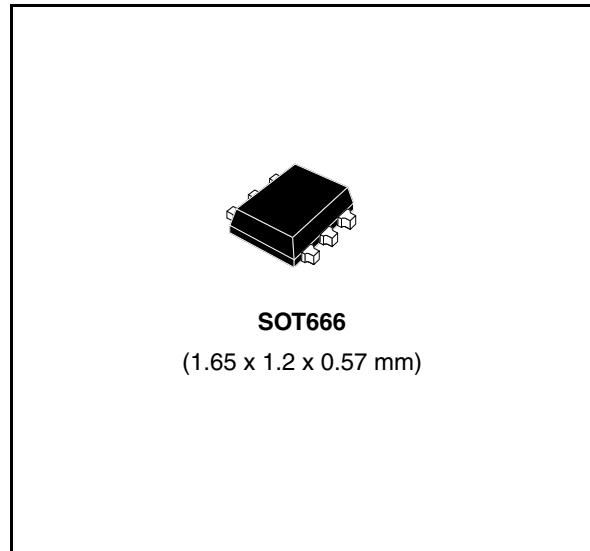
- Power down function
- Integrated matching networks
- Low noise figure 1.15 dB @ 1.575 GHz
- High gain 18 dB @ 1.575 GHz
- High linearity (IIP3 = +3dBm)
- Temperature compensated
- Unconditionally stable
- ESD protection (HBM \pm 2kV)
- 70 GHz Silicon Germanium Technology

Applications

- GPS

Description

The SMA661AS is the first low-noise amplifier with integrated matching networks and embedded power-down function. The chip, which requires only one external input capacitor, drastically reduces the application bill of materials and the PCB area, resulting in an ideal solution for compact and cost-effective GPS LNA.



The SMA661AS, using the ST's leading-edge 70GHz SiGe BiCMOS technology, achieves excellent RF performance at the GPS frequency of 1.575GHz, in terms of power gain, noise Figure and linearity with a current consumption of 8.5mA. The device is unconditionally stable and ESD protected. All these features are steady over the operating temperature range of -40 °C to +85 °C. It's housed in ultra-miniature SOT666 plastic package.

Table 1. Device summary

Part Number	Marking	Package	Packing
SMA661ASTR	661	SOT666	Tape and reel

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1 Pins description and circuit schematic

Table 2. Pins description

Pin No.	Pin Name
1	RF IN
2	GND
3	PD
4	RF OUT
5	GND
6	V _{CC}

Figure 1. Pin connection

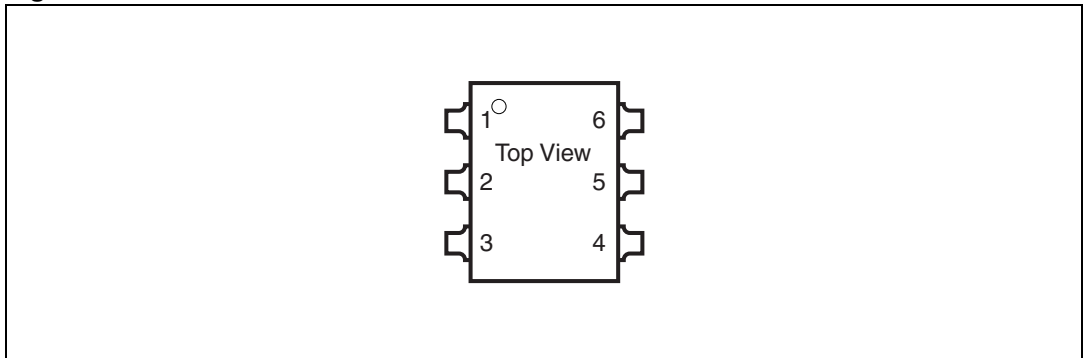
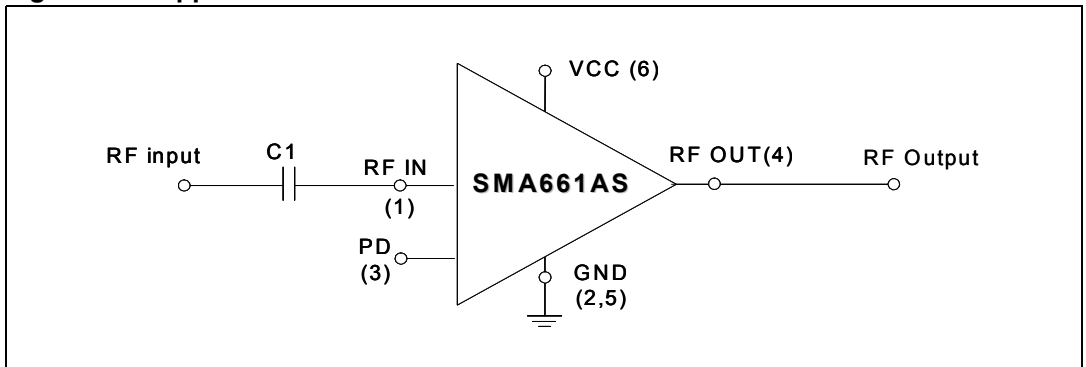


Figure 2. Application circuit schematic



2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Conditions	Value	Unit
V _{CC}	Supply voltage		3.3	V
T _{stg}	Storage temperature		-60 to +150	°C
T _a	Operating ambient temperature		-40 to +85	°C
V _{ESD}	Electrostatic Discharge	HBM (ALL PINs)	± 2000	V
V _{ESD}	Electrostatic Discharge	MM (ALL PINs)	± 200	V

2.2 Electrical characteristics

(T_a = +25 °C, V_{CC} = 2.7 V, Z_L = Z_S = 50 ohm, unless otherwise specified; measured according to [Figure 13](#) at pin level)

Table 4. Electrical characteristics

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Unit
f	Frequency			1575		MHz
V _{CC}	Supply voltage		2.4	2.7	3	V
I _{CC}	Current Consumption			8.5		mA
I _{PD}	Power Down Mode Current Consumption	V _{PD} ≤ V _{PDL}		10		nA
G _p	Power gain			18		dB
NF	Noise figure			1.15		dB
IIP2	Input IP2	f ₁ = 849 MHz, f ₂ = 2424 MHz, P _{in} = -30 dBm		0.5		dBm
IIP3	Input IP3	f ₁ = 1574.5 MHz, f ₂ = 1575.5 MHz, P _{in} = -30 dBm		3		dBm
ISL	Reverse Isolation			-28		dB
RLin	Input Return Loss	f = 1500-1650 MHz		10		dB
RLout	Output Return Loss	f = 1500-1650 MHz		10		dB
V _{PDL} ⁽¹⁾	Power Down Low State				0.5	V
V _{PDH} ⁽²⁾	Power Down High State		1.0			V
Stability		100 - 10000 MHz	Unconditionally stable			

1. The device is switched to OFF state

2. The device is switched to ON state

3 Typical performance

(Vcc = 2.7 V, ZL = ZS = 50 ohm, unless otherwise specified; measured according to [Figure 13](#) at pin level)

Figure 3. Power Gain vs. Frequency

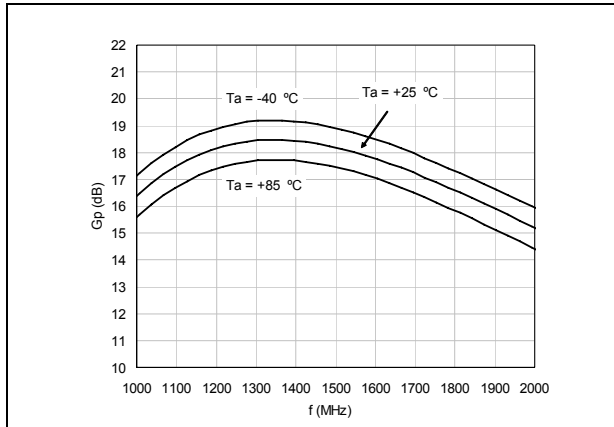


Figure 4. Input Return Loss vs. Frequency

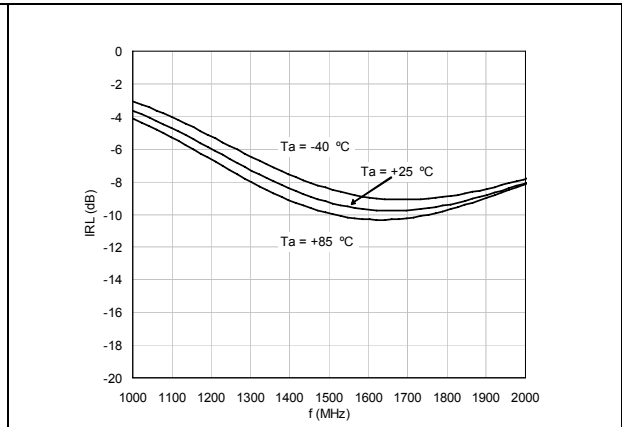


Figure 5. Noise Figure vs. Frequency

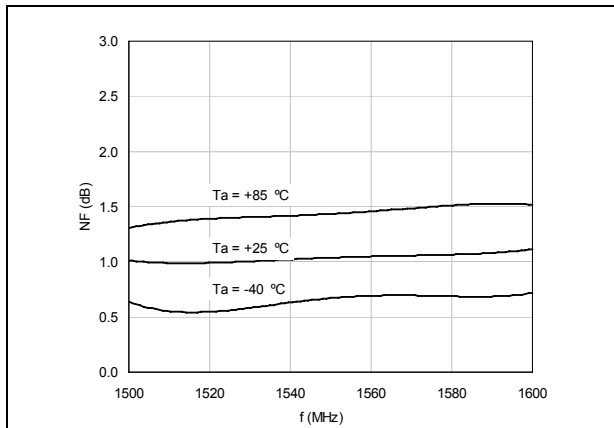


Figure 6. Reverse Isolation vs. Frequency

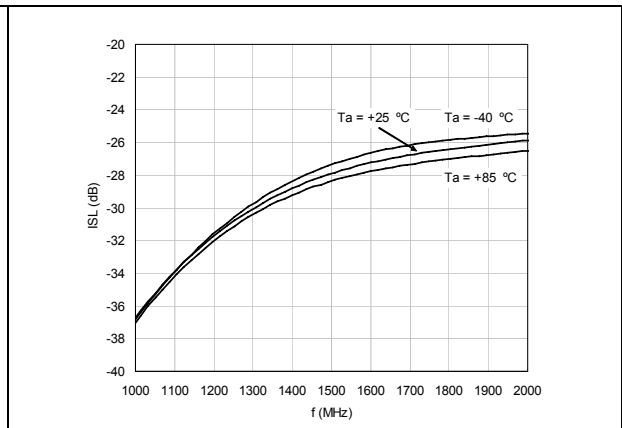


Figure 7. Output Return Loss vs. Frequency

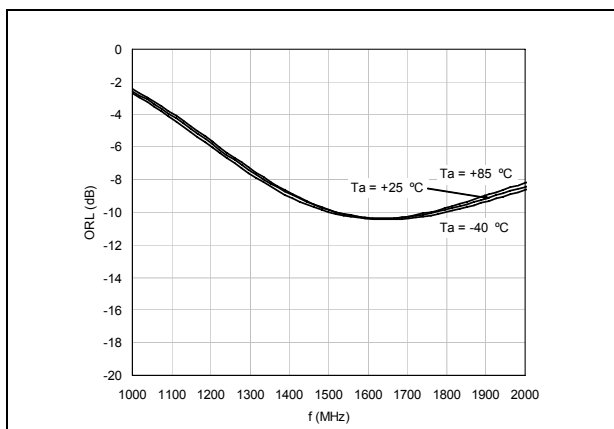


Figure 8. IIP3 vs. Temperature

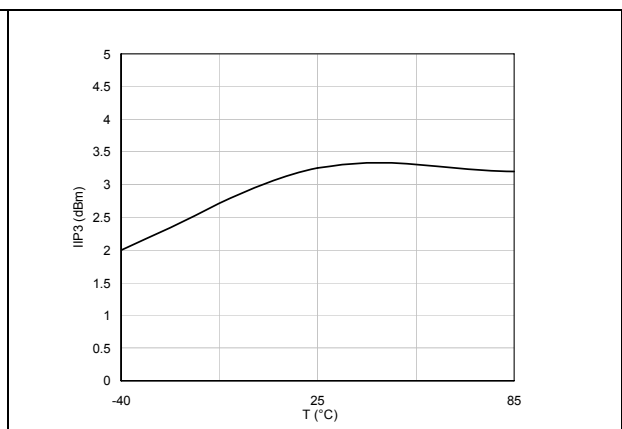


Figure 9. Current Consumption vs. Temperature

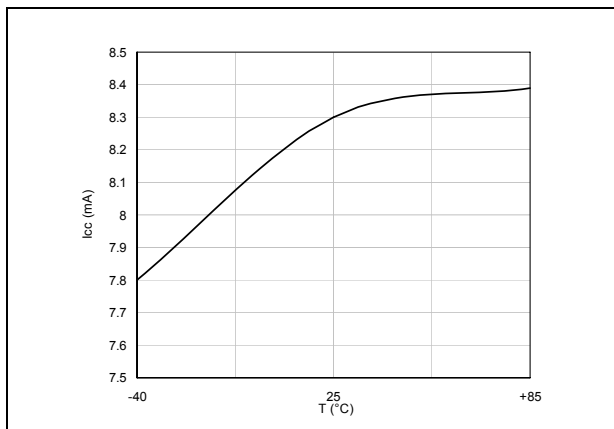


Figure 10. Gain Power Down vs. Temperature

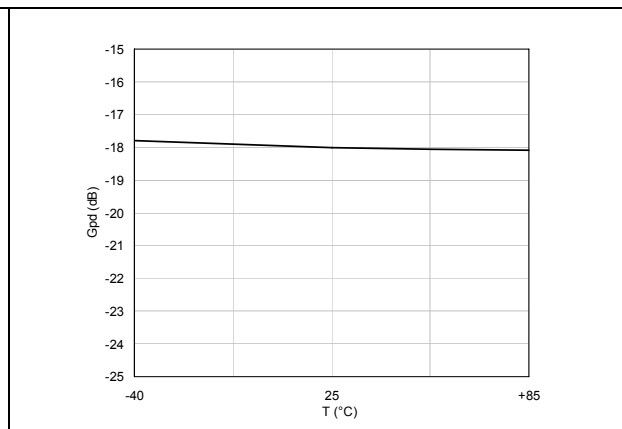
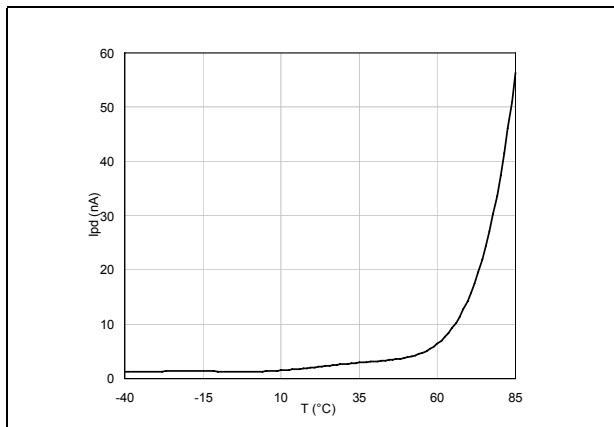
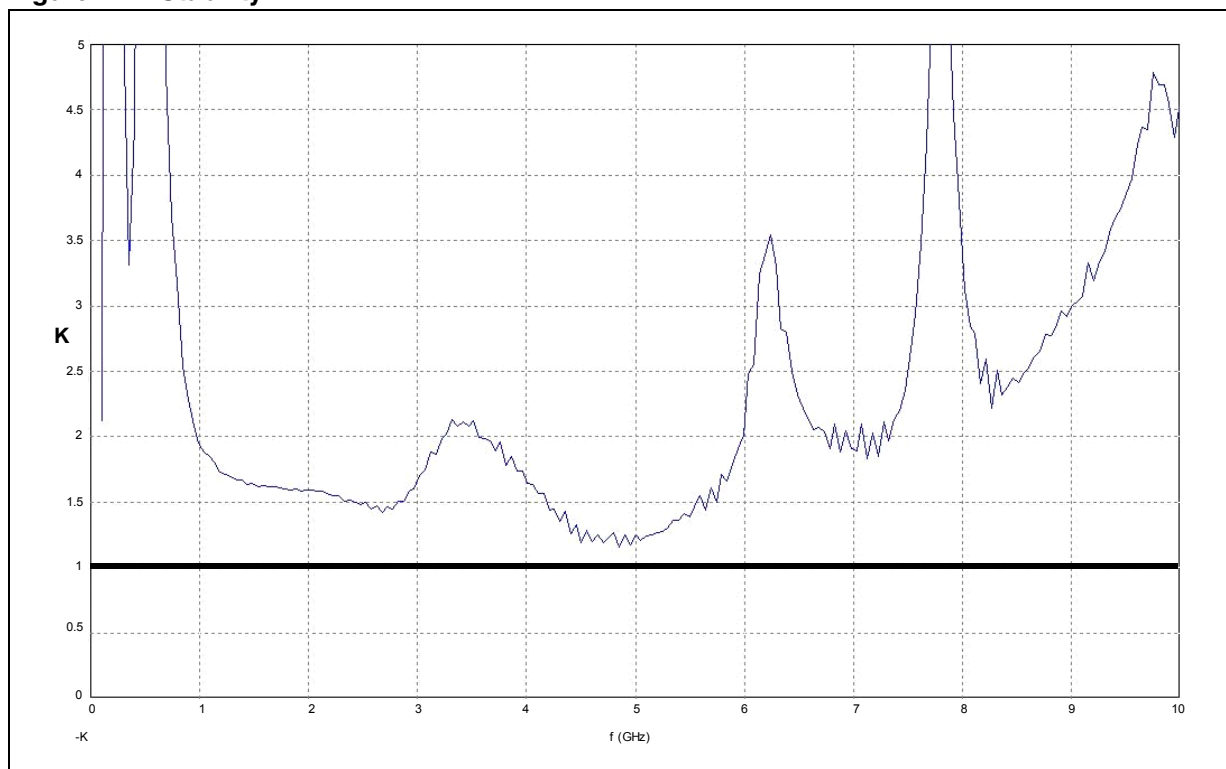


Figure 11. Power Down Current vs. Temperature



Note: S-Parameter are available on request.

Figure 12. Stability



4 Evaluation board description

Figure 13. Evaluation board

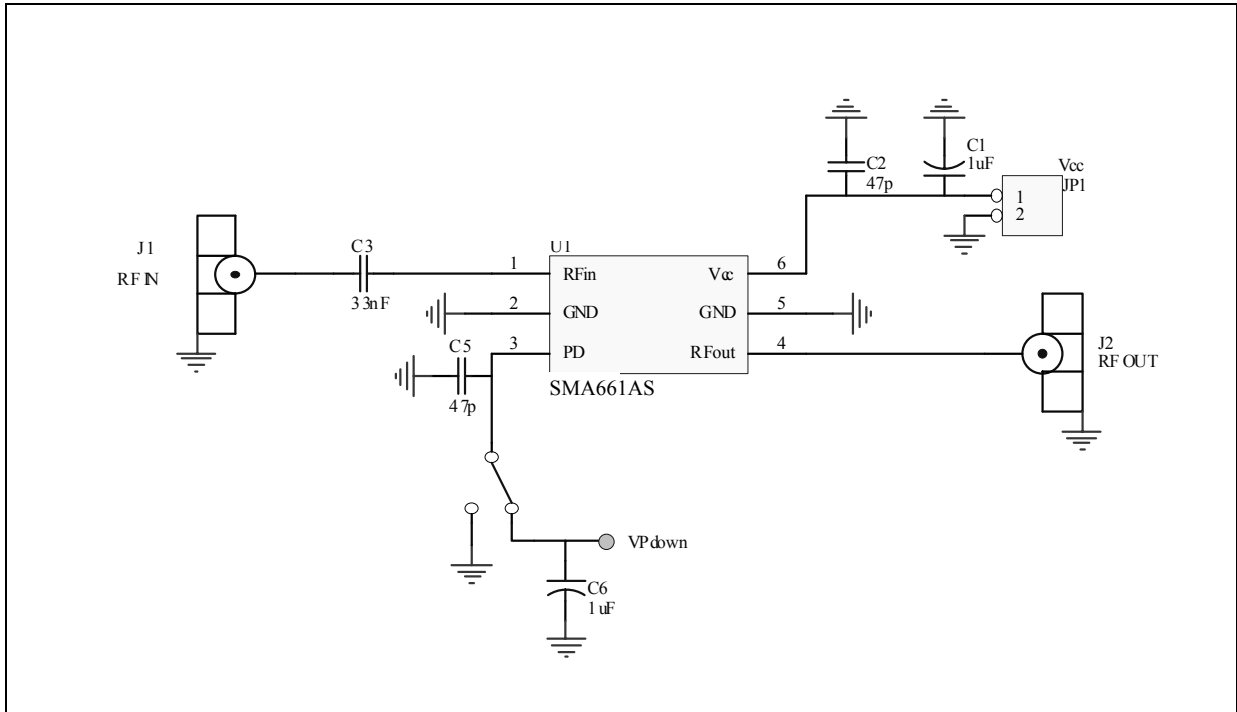


Table 5. Evaluation board bill of material

Component	Value	Type	Manufacturer	Function
C1	1μF (electrolytic)	Case_A	Various	Supply Filter
C2	47 pF	0603	Murata (GRM188)	RF Bypass
C3	33 nF	0603	Murata (GRM188)	Input dc block / IIP3 improvement
C5	47 pF	0603	Murata (GRM188)	RF Bypass
C6	1 μF (electrolytic)	Case_A	Various	Supply Filter
J1	-	142-0711-841 (SMA_Female)	Johnson	RF Input connector
J2	-	142-0711-841 (SMA_Female)	Johnson	RF Output connector
U1	-	SOT666	STMicroelectronics	SMA661AS GPS LNA
Substrate	-	FR4 18mm x 20mm x 1.1mm	Various	Layer = 3 (see Figure 14 & 15)

Figure 14. Evaluation Board Layout

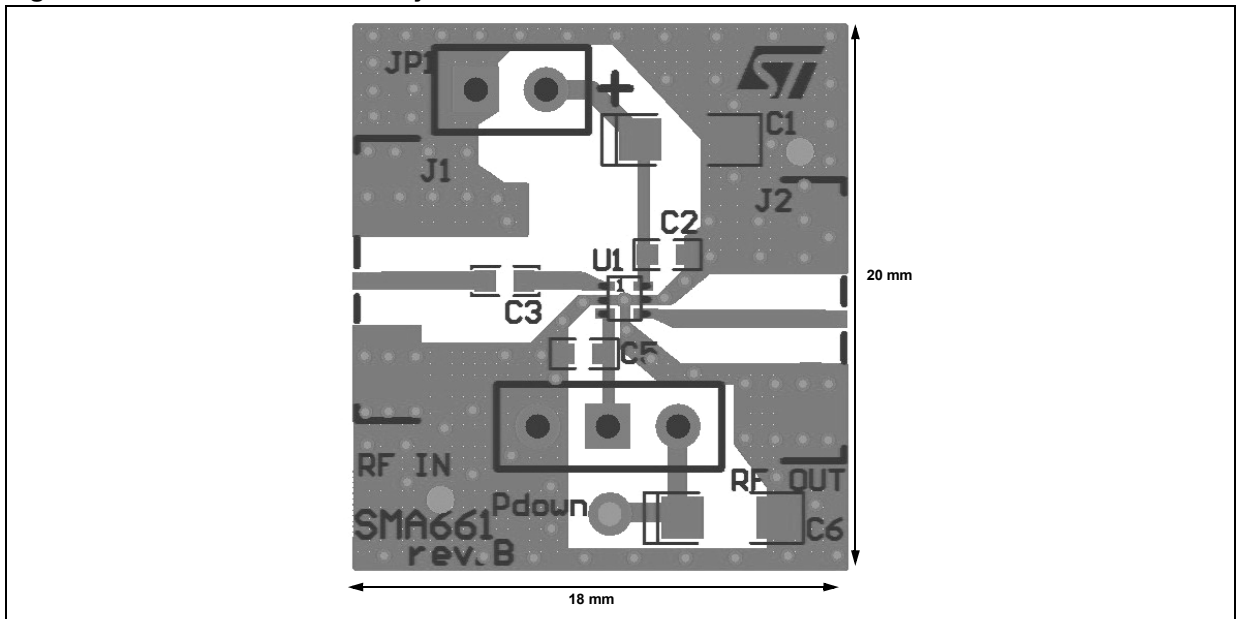
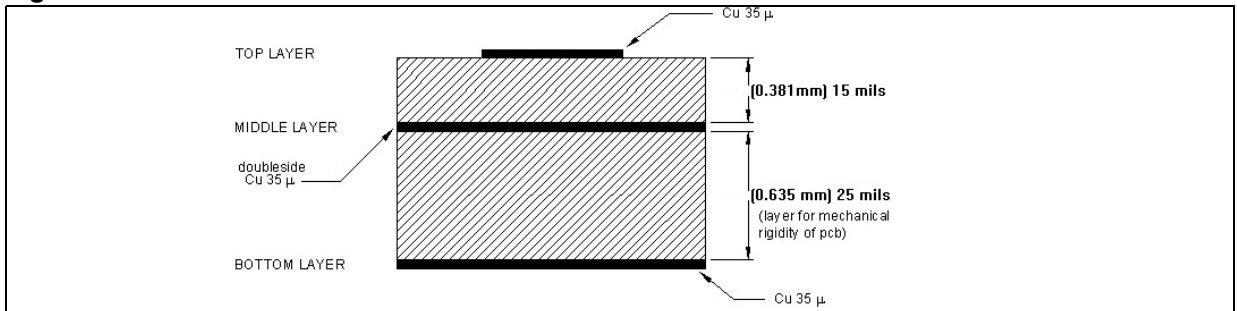


Figure 15. Evaluation Board Cross Section



Note: Gerber files of the SMA661AS evaluation board are available on request.

Layout recommendation:

Both lines from pin 2 and pin 5 to GND plane have to be as short as possible to maximize the performances. Therefore a via hole under the IC is highly recommended.

5 Package and packing informations

5.1 Package informations

In order to meet environmental requirements, ST offers this device in ECOPACK® package. This package has a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

Table 6. SOT666 (Lead-free) mechanical data

DIM.	mm.		
	MIN.	TYP	MAX.
A	0.45		0.60
A3	0.08		0.18
b	0.17		0.27
b1		0.27	0.34
D	1.50		1.70
E	1.50		1.70
E1	1.10		1.30
e		0.50	
L1		0.19	
L2	0.10		0.30
L3		0.10	

Figure 16. SOT666 (Lead-Free) package outline

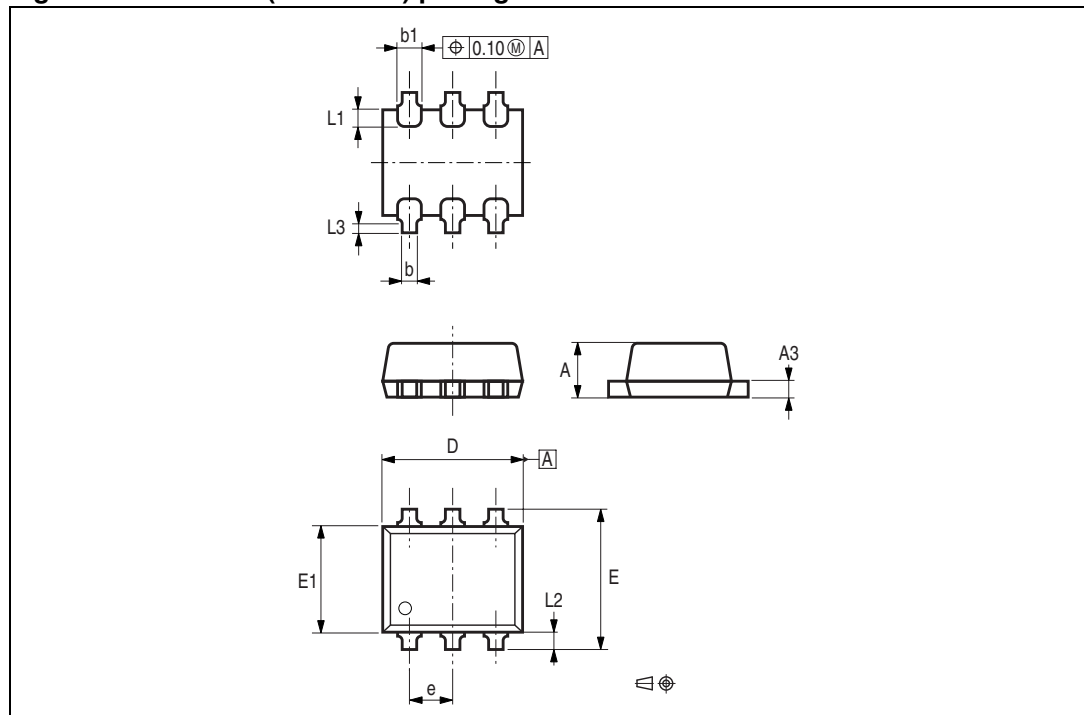
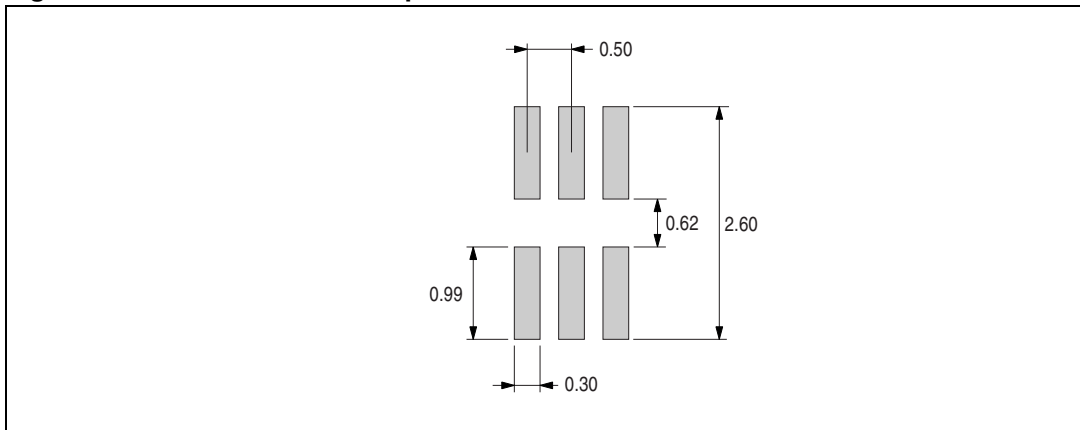


Figure 17. Recommended footprint



5.2 Packing informations

Figure 18. Reel description

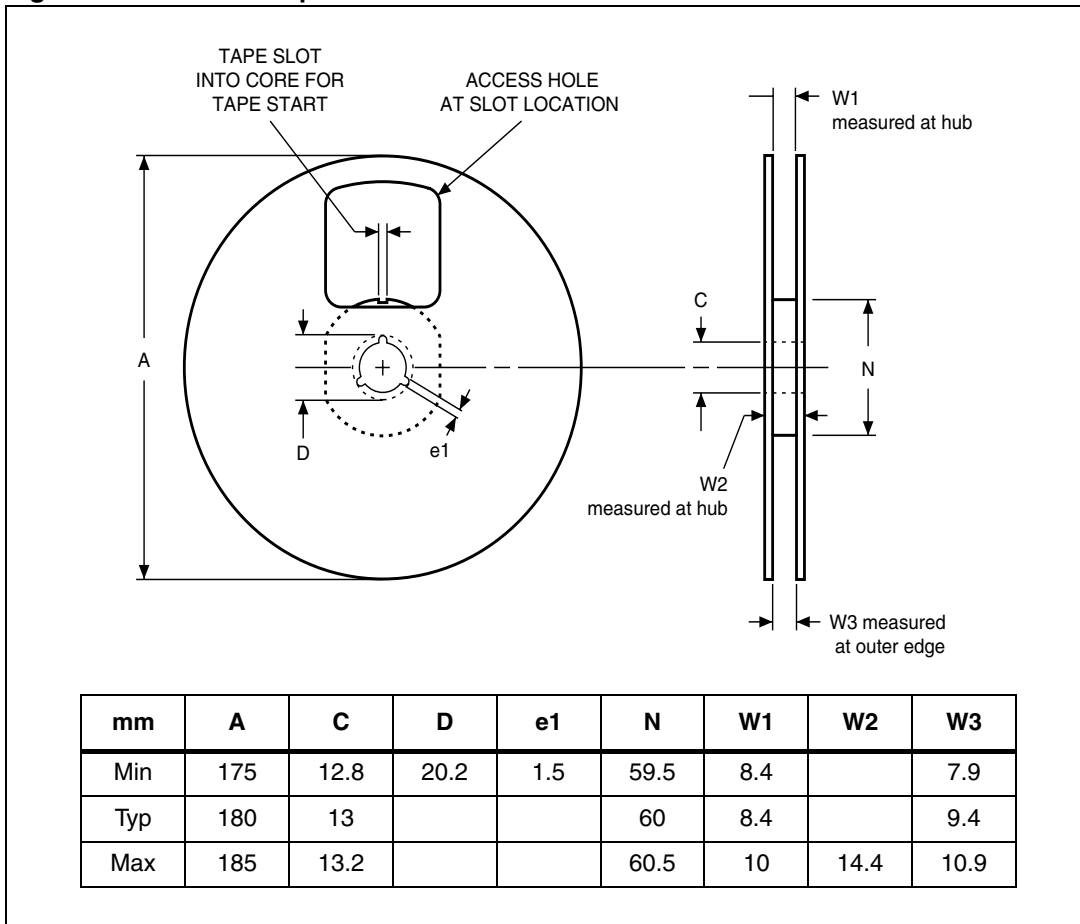


Figure 19. Carrier tape requirements

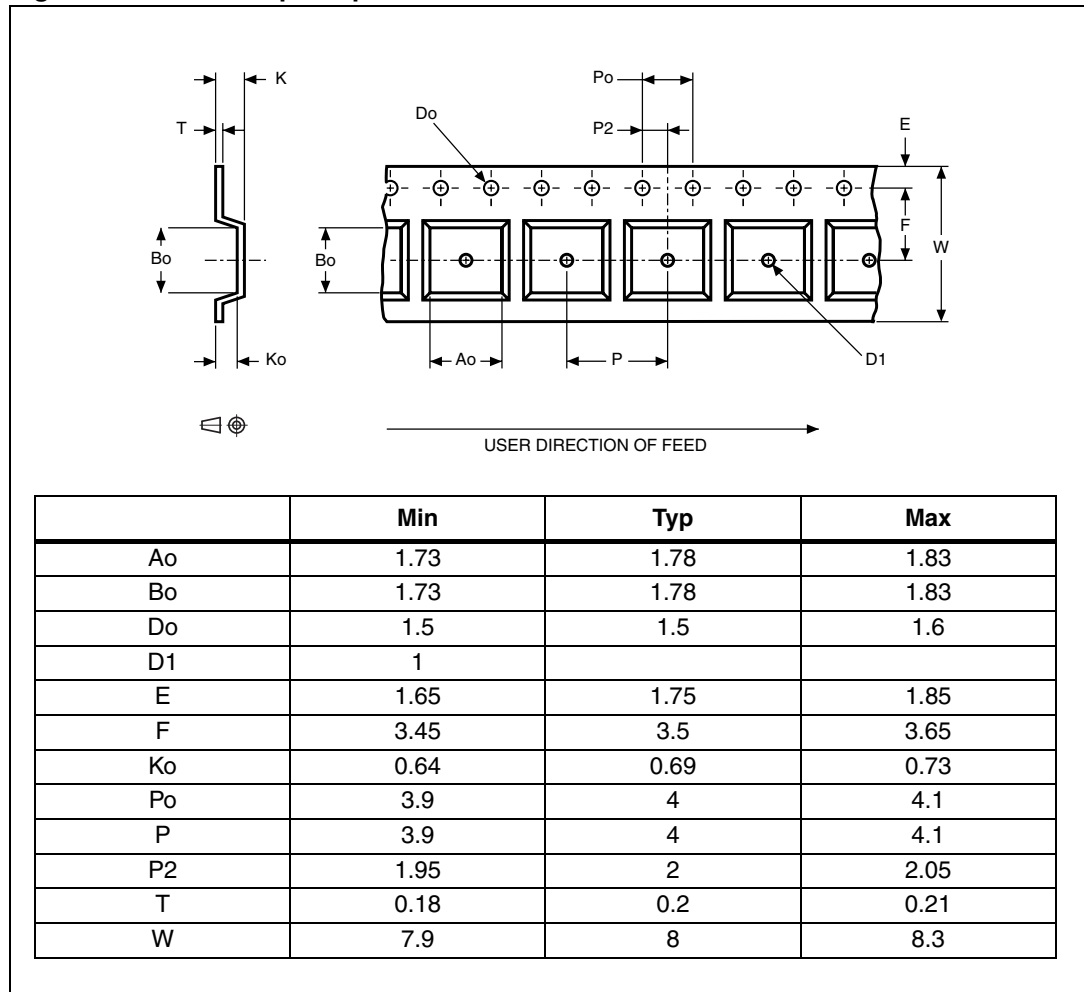
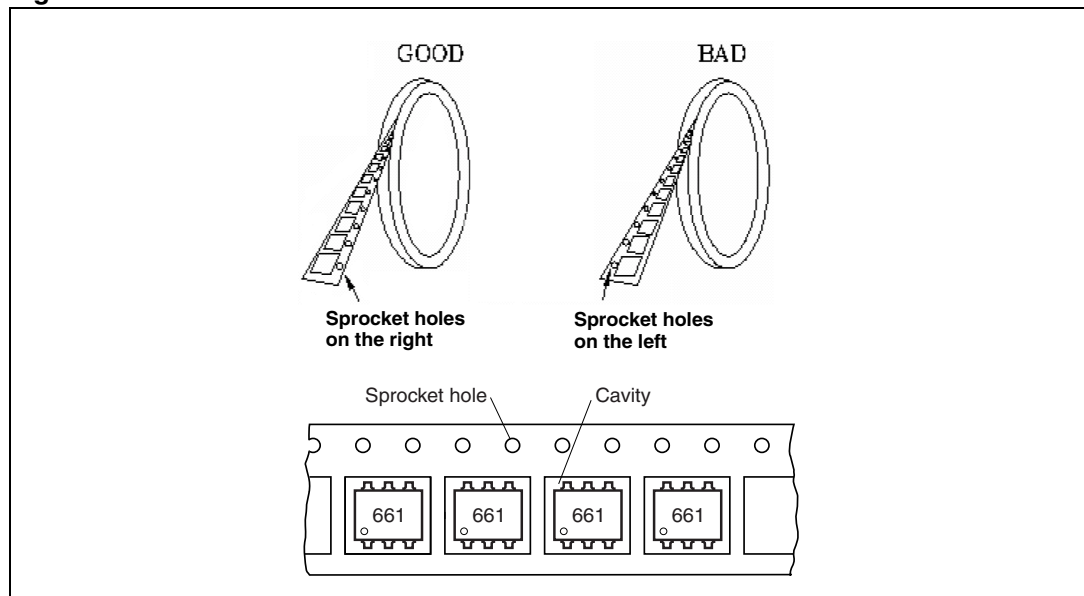


Figure 20. Device orientation



6 Revision history

Table 7. Document revision history

Date	Revision	Changes
15-Jul-2005	1	Initial release.
20-Oct-2005	2	Added: Evaluation Board Schematic & Layout.
07-Jul-2006	3	Changed to new template. Added packing informations.
04-Apr-2007	4	Updated noise figure and high gain values. Updated Figure 3 and Figure 5 .

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